REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 7-11 are pending in the present application. Claims 7-11 are amended by the present amendment. Claims 1-6 and 12-27 were previously canceled.

In the outstanding Office Action, Claim 7 was objected to because of informalities; Claim 9 was rejected under 35 U.S.C. § 103(a) as unpatentable over JP 10-042181 to Yoshihiro in view of U.S. Patent No. 5,784,100 to Konishi; Claim 7 was rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshihiro in view of U.S. Patent No. 5,905,533 to Hidari; and Claims 8, 10, and 11 are allowed.

Applicants thank the Examiner for the indication of allowability of Claims 8, 10, and 11.

Regarding the objection to Claim 7, Claim 7 is amended to remove the informality identified in the Office Action. Accordingly, it is respectfully requested the objection to Claim 7 be withdrawn.

Applicants respectfully traverse the rejection of Claim 9 under 35 U.S.C. § 103(a) as unpatentable over Yoshihiro and Konishi.

Claim 9 is directed to an image processing circuit configured to perform a predetermined image processing of pixel data in an image photographed by an image pickup device. The circuit includes, in part, a real time processing unit configured to sequentially input the pixel data photographed by the image pickup device, perform, by real time processing, a predetermined general image processing of the inputted pixel data, and output the generally processed pixel data. The circuit also includes a main memory configured to store the generally processed pixel data outputted from the real time processing unit, in image frame units. Further, the circuit includes a central control unit configured to execute

exceptional image processing as a software program processing with respect to the stored generally processed pixel data, and store the exceptionally processed pixel data in the main memory.

The real time processing unit also includes a pixel compensation function, including a shading compensation, in which each pixel data inputted sequentially is multiplied by a predetermined pixel compensation parameter previously stored in the main memory.

Applicants respectfully submit that Yoshihiro and Konishi, whether taken individually or in combination, fail to teach or suggest each of the features of Claim 9. For example, Yoshihiro and Konishi fail to teach or suggest a real time processing unit having a pixel compensation function in which pixel data is multiplied by a predetermined pixel compensation parameter previously stored in a main memory that is configured to store generally processed pixel data outputted from the real time processing unit.

Yoshihiro describes a camera in which a prescribed signal processing may be conducted by a digital signal processing section 5.[1] Further, Yoshihiro indicates that a DRAM 6 (e.g., main memory) may be used to read and write various image data while various image processings are performed.[2] Further, Yoshihiro indicates that a real time processing may include an automatic white balance compensation function. However, Applicants respectfully submit that Yoshihiro fails to teach or suggest any predetermined compensation parameter previously stored in the DRAM 6 that is multiplied by each pixel data. Further, Applicants respectfully traverse the assertion in the outstanding Office Action that Yoshihiro discloses a pixel compensation function including multiplication by a predetermined pixel compensation parameter at paragraphs [0049] and [0066].[3] On the other hand, in the cited paragraphs, Yoshihiro merely indicates that the "AWB system computes the amendment data of a white balance by repeating reading of the colorimetry data of a 8

[1] Yoshihiro at Abstract.
[2] Yoshihiro at paragraph [0024].
[3] Office Action at page 3, last paragraph to page 4, line 4.

above-mentioned blocks field 5 times."[4] In other words, Yoshihiro indicates that colorimetry data of plural blocks of pixels is repeatedly read as part of the AWB function. However, Yoshihiro fails to indicate that the colorimetry data is stored in DRAM 6 or that the colorimetry data is multiplied by each pixel data inputted sequentially, as required by Claim 9.

Further, in cited paragraph [0066], Yoshihiro indicates that "required data are computed by AF-AE-AWB etc." and "computer data lets the data interface section 20 and the ADD bus 12 pass by serial communication link, and is sent to MPU3. In other words, when MPU3 is required, it reads. Therefore, the setting preparations for it are made at step 206." Thus, Yoshihiro indicates that the MPU3 may read computed data as required. However, as explained above, Yoshihiro again fails to teach or suggest any predetermined pixel compensation parameter previously stored in main memory that is multiplied by each pixel data.

Further, as admitted in the Office Action at page 4, lines 5-6, Yoshihiro fails to disclose a predetermined pixel compensation including shading compensation, and asserts that feature is taught by Konishi. However, Applicants respectfully submit that Konishi also fails to teach or suggest a pixel compensation function in which each pixel data inputted sequentially is multiplied by a predetermined pixel compensation parameter previously stored in a main memory.

Konishi describes an apparatus for performing a shading correction in which data representing a differential correction factor which is equal to the difference between shading correction factors for adjacent pixels is previously stored for each pixel in a differential correction factor memory 12.[5] However, the differential correction factor memory 12 of Konishi is a memory used only for the storage of differential correction factor and is not a

[4] Yoshihiro at paragraph [0049].
[5] Konishi at column 4, lines 12-15 and 28-34.

memory used to store pixel data outputted from a real time processing unit or a main memory configured to store exceptionally processed pixel data, as in Claim 9. Accordingly, the differential correction factor of Konishi is also not stored in a main memory.

Accordingly, Applicants respectfully submit that Yoshihiro and Konishi, whether taken individually or in combination, fail to teach or suggest an image processing circuit that includes a main memory configured to store pixel data outputted from a real time processing unit, which comprises a pixel compensation function "in which each pixel data inputted sequentially is multiplied by a predetermined pixel compensation parameter previously stored in said main memory," as recited in independent Claim 9.

Accordingly, Applicants respectfully submit that independent Claim 9 and claims depending therefrom are allowable.

In addition, Applicants respectfully traverse the rejection of Claim 7 as unpatentable over Yoshihiro in view of Hidari.

Claim 7 is directed to an image processing circuit including, in part, a real time processing unit, a main memory, and a central control unit. Applicants respectfully submit that Yoshihiro and Hidari, whether taken individually or in combination, fail to teach or suggest each of the features of independent Claim 7. For example, Yoshihiro and Hidari, fail to teach or suggest a real time processing unit that is configured to perform a cumulative addition processing function in which a pixel data residing on a same position and a preceding frame of pixel data stored in the main memory is added to a corresponding pixel data in each frame inputted sequentially when the pixel data inputted sequentially extends multiple frames. First, as noted in the Office Action, Yoshihiro fails to teach or suggest those features.[6]

[6] Office Action at page 4, last paragraph, to page 5, line 4.

In addition, Hidari also fails to teach or suggest a real time processing unit configured to perform a cumulative addition processing function that stores results in a main memory configured to store generally processed pixel data and exceptionally processed pixel data. Hidari indicates that a latest still image data is added to a past still image data and the result is stored in an image memory 24. Hidari indicates "[t]he image memory is an 8-bit memory which stores the integrated still image data."[7] Further, Hidari indicates that controller 26 is a system controller that controls image memory 24 and palette RAM 25 to receive the proper stop value and the stopped-down value.[8] In addition, as shown in Figs. 2, 11, and 12, the controller 26 of Hidari is configured to control the contents of the palette RAM 25 based on a stop value step a and to control a number of iterations of the repeated adding. In addition, Hidari does not teach or suggest any exceptional image processing performed as a software program processing, which stores exceptionally processed pixel data in a main memory. Thus, according to Hidari the image memory 24 is dedicated to receiving image data from adder 23 and providing data to RAM 25 under the control of controller 26. However, the image memory of Hidari is not a main memory that is configured to store generally processed image data and exceptionally processed image data, and Hidari does not teach or suggest those features.

Accordingly, Applicants respectfully submit that Yoshihiro and Hidari, whether taken individually or in combination, fail to teach or suggest an image processing circuit having a control unit configured to store exceptionally processed data in a main memory, and a real-time processing unit configured to store exceptionally processed data in the main memory, where the real-time processing unit is configured to perform a cumulative addition processing function configured to "store results of the cumulative addition processing function in said main memory," as recited in independent Claim 7.

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[7] Hidari at column 5, lines 49-50.
[8] Hidari at column 6, lines 5-8.

Accordingly, Applicants respectfully submit that independent Claim 9 and claims depending therefrom are also allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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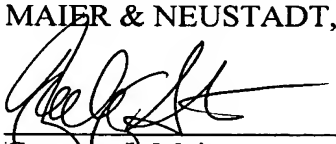

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